FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **212771US22PCT**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/926186

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/01736	**22 March 2000**	**25 March 1999**

TITLE OF INVENTION
SEMICONDUCTOR DEVICE

APPLICANT(S) FOR DO/EO/US
KAWASAKI Masashi et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Request for Consideration of Documents Cited in International Search Report
Notice of Priority
Drawings (15 Sheets)

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/926186	PCT/JP00/01736	212771US22PCT

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$1000.00**
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	**$860.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$710.00**
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$690.00**
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$130.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	21 - 20 =	1	x $18.00	**$18.00**	
Independent claims	2 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$1,008.00**	
☐ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$1,008.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$1,008.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
TOTAL FEES ENCLOSED =				**$1,008.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$1,008.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

22850

Surinder Sachar
Registration No. 34,423

Surinder Sachar
SIGNATURE

Richard A. Neifeld
NAME

35,299
REGISTRATION NUMBER

Sept. 20 2001
DATE

212771US-22 PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

MASASHI KAWASKI ET AL : ATTN: APPLICATION DIVISION

SERIAL NO: NEW US PCT APPLN :
(Based on PCT/JP00/01736)

FILED: HEREWITH : EXAMINER:

FOR: SEMICONDUCTOR DEVICE :

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 1-10.

Please add new Claims 11-30 as follows:

11. (New) A semiconductor device comprising,

a substrate containing a material of formula $LnABO_4$ or $LnAO_3(BO)_n$ for basic structure,

wherein,

Ln is a rare earth element,

A is selected from the group consisting of Fe, Ga and Al,

B is selected from the group consisting of Mn, Co, Fe, Zn, Cu, Mg and Cd,

and,

a semiconductor layer formed on said substrate,

wherein said semiconductor layer is formed from a group II metal oxide.

12. (New) The semiconductor device claimed in Claim 11,

wherein Ln is selected from the group consisting of Sc, In, Lu, Yb, Tm, Ho, Er and Y.

13. (New) The semiconductor device as claimed in Claim 11,

wherein the group II metal oxide is selected from the group consisting of zinc oxide (ZnO), zinc magnesium oxide ($Mg_xZn_{1-x}O$), zinc cadmium oxide ($Cd_xZn_{1-x}O$) and cadmium oxide (CdO).

14. (New) The semiconductor device according to claim 11,

wherein said substrate is a material selected from the group consisting of $ScA1MgO_4$, $ScA1ZnO_4$, $ScAlCoO_4$, $ScAlMnO_4$, $ScGaZnO_4$, $ScGaMgO_4$, $ScAlZn_3O_6$, $ScAlZn_4O_7$, $ScAlZn_7O_{10}$, $ScGaZn_3O_6$, $ScGaZn_5O_8$, $ScGaZn_7O_{10}$, $ScFeZn_2O_5$, $ScFeZn_3O_6$ and $ScFeZn_6O_9$,

and,

ZnO is used as a material for said semiconductor layer.

15. (New) The semiconductor device according to claim 11,

wherein said substrate is a material selected from the group consisting of $ScAlO_3(ZnO)_n$, $ScFeO_3(ZnO)_n$, $ScGaO_3(ZnO)_n$, $InFeO_3(ZnO)_n$, $InGaO_3(ZnO)_n$, $InAlO_3(ZnO)_n$, $YbA1O_3(ZnO)_n$ and $LuAlO_3(ZnO)_n$,

and,

ZnO is used as a material for said semiconductor layer.

16. (New) A semiconductor device comprising,

a substrate containing a material selected from the group consisting of $ScAlBeO_4$, $ScBMgO_4$, $ScBBeO_4$ and $1nAO_3(MgO)_n$,

wherein A is selected from the group consisting of Fe, Ga and Al,

B is selected from the group consisting of Mn, Co, Fe, Zn, Cu, Mg and Cd, and

a semiconductor layer formed on said substrate from a material selected from the group consisting of GaN, AlN, InGaN and AlInN.

17. (New) The semiconductor device according to claim 11,

further comprising a buffer layer, between said substrate and said semiconductor layer,

wherein said buffer layer contains a material having a composition or a structure identical to that of said semiconductor layer as a base and slightly doped or undoped with impurities.

18. (New) The semiconductor device according to claim 17,

wherein ZnO is used for said semiconductor layer, and

said buffer layer is an insulating material slightly doped with an element capable of taking valence of 1 value or a group V element, an insulating semiconductor containing undoped and pure insulating ZnO or a combination thereof.

19. (New) The semiconductor device as claimed in claim 18,

wherein said buffer layer is ZnO.

20. (New) The semiconductor device according to Claim 11,

further comprising an insulating layer formed by using a material identical to that for said substrate for a basic structure.

21. (New) The semiconductor device according to claim 11,

further comprising a light emission layer formed on said semiconductor layer by using a material having a composition or a structure identical to that of said semiconductor layer as a base, and

a second semiconductor layer which is formed on said light emission layer by using a material having a composition or a structure identical to that of said semiconductor layer as a base, and which has a different channel from that of said semiconductor layer.

22. (New) The semiconductor device according to claim 21,

wherein said light emission layer is selected from the group consisting of a multilayer structure of (Mg, Zn)O and ZnO, a multilayer structure of (Zn, Cd)O and ZnO, and a multilayer structure of (Mg, Zn)O and (Zn, Cd)O.

23. (New) The semiconductor device according to claim 11,

wherein said semiconductor layer is an insulating semiconductor,

input and output electrodes are further formed on said semiconductor layer, and

a filter characteristic is provided.

24. (New) The semiconductor device according to claim 16,

further comprising a buffer layer, between said substrate and said semiconductor layer,

wherein said buffer layer contains a material having a composition or a structure identical to that of said semiconductor layer as a base and slightly doped or undoped with impurities.

25. (New) The semiconductor device according to claim 24,

wherein ZnO is used for said semiconductor layer, and

said buffer layer is an insulating material slightly doped with an element capable of taking valence of 1 value or a group V element, an insulating semiconductor containing undoped and pure insulating ZnO, or a combination thereof.

26. (New) The semiconductor device as claimed in claim 25,

wherein said buffer layer is ZnO.

27. (New) The semiconductor device according to Claim 16,

further comprising an insulating layer formed by using a material identical to that for said substrate for a basic structure.

28. (New) The semiconductor device according to claim 16,

further comprising a light emission layer formed on said semiconductor layer by using a material having a composition or a structure identical to that of said semiconductor layer as a base, and

a second semiconductor layer which is formed on said light emission layer by using a material having a composition or a structure identical to that of said semiconductor layer as a base, and which has a different channel from that of said semiconductor layer.

29. (New) The semiconductor device according to claim 28,

wherein said light emission layer is selected from the group consisting of a multilayer structure of (Mg, Zn)O and ZnO, a multilayer structure of (Zn, Cd)O and ZnO, and a multilayer structure of (Mg, Zn)O and (Zn, Cd)O.

30. (New) The semiconductor device according to claim 16,

wherein said semiconductor layer is an insulating semiconductor,

input and output electrodes are further formed on said semiconductor layer, and

a filter characteristic is provided.

REMARKS

Claims 11-30 are active in the present application. The original claims have been amended to remove multiple dependencies, for clarity, and to conform to U.S. Patent Practice. No new matter is added. An action on the merits and allowance of the claims is solicited.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Norman F. Oblon
Attorney of Record
Registration No. 24,618

Daniel J. Pereira
Registration No. 45,518

22850

(703) 413-3000
Fax #: (703)413-2220
DJPER/rac
I:\atty\SUKOS\212771US-PR.wpd

Marked-Up Copy
Serial No: _____
Amendment Filed on:
9-20-01

IN THE CLAIMS

Claims 1-10 (Cancelled).

Claims 11-30 (New).

I:\atty\SUKOS\212771US-PR.wpd

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

The present invention relates to a semiconductor device. More particularly, the invention relates to a semiconductor device having a high quality single crystal thin film formed by using group II oxide or group III nitride as a thin film material, and an oxide single crystal having good lattice compatibility with the thin film material for a substrate. The invention also relates to the application of such a semiconductor device to a light emission device, a surface acoustic wave (SAW) device, or the like.

BACKGROUND ART

Heretofore, in the semiconductor device, for example, as a transistor, a thin film transistor using amorphous silicon, polycrystal silicon or the like has been utilized. Recently, focus of attention has been placed on zinc oxide (ZnO) to be used as a thin film material for manufacturing the semiconductor device. Not only an ultraviolet ray emission device, a transparent transistor, and so on, have replaced the existing application as photo-electron devices, but also totally new applications have been developed. Currently, for manufacturing a light emission device or a transistor using ZnO, a sapphire substrate is used.

In addition, heretofore, for manufacturing the semiconductor device, the formation of a high quality thin film on the substrate has been much requested.

The following factors may conceivably determine the quality of thin film crystallinity (coherency):

(a) grain size;

(b) fluctuation of lattice plane spacing (distortion); and

(c) fluctuation of lattice plane direction (orientation, mosaicness).

Generally, a high quality crystal is characterized by (a) a large grain size, (b) small fluctuation of lattice plane spacing, and (c) small mosaicness.

DISCLOSURE OF THE INVENTION

However, in the conventional substrate using sapphire or the like, lattice mismatching with ZnO as a thin film material was large, reaching approximately 18%. Consequently, a grain boundary existed or mosaicness was increased to make it difficult to form a high quality single crystal thin film. In addition, conventionally, with regard to device performance, the intrinsic performance of ZnO was not placed into full play, making it impossible to always manufacture an optimal substrate.

The present invention was made to solve the foregoing problems. It is an object of the invention to manufacture a semiconductor device with superior characteristics by using an oxide crystal having very high lattice compatibility with a thin film material such as group II oxide, e.g., ZnO or group III nitride, e.g., GaN, for a substrate, thereby increasing the quality of the thin film material, and then forming a high quality thin film comparable to a bulk single crystal. It is another object of the invention to form a semiconductor thin film of ZnO, GaN or the like, having almost no grain

boundaries, a large grain size, small fluctuation of lattice plane spacing, very small mosaicness, and a high quality nearly comparable to a single crystal.

According to the invention, for example, since lattice mismatching of an $ScAlMgO_4$ (SCAM) crystal or the like with ZnO is small (approximately 0.13%), an object is to form a ZnO thin film of nearly a single crystal on a substrate. Another object according to the invention is to form ZnO on the SCAM substrate having higher electron mobility and more comparable to a ZnO single crystal compared with that of the conventional sapphire substrate or the like.

According to the invention, an object is to manufacture a transparent semiconductor device by combining a transparent semiconductor material of ZnO with a transparent and highly insulating SCAM substrate, and greatly improve the performance of a heterostructured device.

An object is to achieve a high switching speed by applying the invention to a transistor or the like. In addition, an object is to lower a gate voltage for switching by applying the invention to a field effect transistor so as to obtain a wider depletion layer when an electric field is applied. Another object is to increase light emission efficiency by applying the invention to a light emission device.

An object is to improve the performance of various electron devices by applying the invention to the devices including a field effect transistor, a bipolar transistor, a light emission device containing a GaN based nitride blue laser (LED, laser), a surface acoustic wave (SAW) device, a sensor or the like.

In accordance with first solving means of the invention, a semiconductor device is provided, comprising: a substrate using a material containing one selected from $LnABO_4$ and $LnAO_3(BO)_n$ for a basic structure (Ln: rare earth element selected from Sc, In, Lu, Yb, Tm, Ho, Er, Y or the like, A: selected from Fe, Ga and Al, and B: selected from Mn, Co, Fe, Zn, Cu, Mg and Cd); and a semiconductor layer formed on the substrate by using a material selected from the group II oxides including zinc oxide ZnO, zinc magnesium oxide $Mg_xZn_{1-x}O$, zinc cadmium oxide $Cd_xZn_{1-x}O$, cadmium oxide CdO, and so on, and the group III nitrides including gallium nitride GaN, aluminum nitride AlN, indium nitride InN, and so on.

Further, in accordance with the invention, a semiconductor device is provided, which is applied to a photo-electronic device such as a light emission device, a SAW device or the like.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are sectional views, each of which shows a semiconductor device according to a first embodiment of the present invention.

Fig. 2 is a view showing an example of a representative thin film material used for a channel layer, and a lattice constant thereof.

Fig. 3 is a view showing a relation between a lattice constant and an ionic radius regarding $LnABO_4$.

Fig. 4 is a view showing an example of a substrate material using $LnABO_4$ for a basic structure, and a lattice constant thereof.

Fig. 5 is a view showing a relation between a lattice constant and an ionic radius regarding $LnAO_3(BO)_n$.

Figs. 6A and 6B are sectional views, each of which shows a semiconductor device according to a second embodiment of the invention.

Fig. 7 is a view illustrating comparison in electric characteristics between a zinc oxide thin film and a zinc oxide bulk single crystal.

Fig. 8 is a view illustrating comparison in X-ray reciprocal lattice mapping between the zinc oxide thin film and the zinc oxide bulk single crystal.

Fig. 9 is a comparative view illustrating dependence of a half value width of an X-ray rocking curve on a substrate temperature.

Fig. 10 is a comparative view illustrating flatness of a thin film surface.

Fig. 11 is a comparative view illustrating dependence of nitrogen concentration on the substrate temperature.

Figs. 12A and 12B are sectional views, each of which shows a semiconductor device according to a third embodiment of the invention.

Fig. 13 is a sectional view showing a semiconductor device according to a fourth embodiment of the invention.

Fig. 14 is a sectional view showing a semiconductor device according to a fifth embodiment of the invention.

Figs. 15A and 15B are constitutional views, each of which shows a semiconductor device according to a sixth embodiment of the invention.

BEST MODES OF CARRYING OUT THE INVENTION

(1) Field Effect Transistor (FET)

Figs. 1A and 1B are sectional views, each of which shows a semiconductor device according to the first embodiment of the invention. As shown in Fig. 1A, the semiconductor device of the first embodiment is for an FET, and comprises: a channel layer (semiconductor layer) 11; a source 12; a drain 13; a gate 14; a gate insulating layer 15; and a substrate 16. The channel layer 11 is formed on the substrate 16. On the channel layer 11, the gate insulating layer 15, the source 12, and the drain 13 are formed. The gate 14 is formed on the gate insulating layer 15.

Fig. 1B specifically shows a modified example of the first embodiment. This transistor includes the channel layer 11 formed on the substrate 16. Further, on the channel layer 11, the source 12 and the drain 13 are formed by ohmic junction, and the gate 14 is formed by Schottky junction. In this example, since the gate insulating layer 15 does not exist unlike the case shown in Fig. 1A, proper spacing is set between the source 12/drain 13 and the gate 14.

Next, description will be made of materials for components, which are the main features of the invention.

First, the channel layer 11 is formed of a proper conductive or insulating semiconductor based on an FET structure. As a material to be used for the channel layer 11, other than a widely known semiconductor material, one can be selected from group II oxides including, e.g., zinc oxide ZnO, zinc magnesium oxide $Mg_xZn_{1-x}O$, zinc cadmium oxide $Cd_xZn_{1-x}O$, cadmium oxide CdO, and so on. For the channel layer 11, one selected

from group III nitrides including gallium nitride GaN, aluminum nitride AlN, indium nitride InN, InGaN, AlInN, and so on, can be used. For the channel layer 11, an undoped and pure or nearly pure thin film material is used. For the channel layer 11, one made of a doped material may also be used. In addition, these thin film materials maybe n or p type.

Fig. 2 shows an example of a representative thin film material used for the channel layer, and the lattice constant thereof. The description will be made by way of example of materials shown. But there should be no limitation placed in this regard.

An insulating material is used for the substrate 16. In the invention, a high quality channel layer 11 was formed by using a highly compatible material to have a lattice constant approximated to the lattice constant of the channel layer 11. For example, if ZnO is used for the channel layer 11, by using one of the highest performance materials, e.g., a zinc oxide single crystal or an $ScAlMgO_4$ single crystal, for the substrate 16, the channel layer 11, the source 12, the drain 13, and so on, can be formed on the substrate by means of epitaxial growth.

Next, description will be made of a combination example of a material for the substrate 16 having high compatibility (i.e., having a lattice constant approximated to that of a thin film material) with the lattice constant of the thin film material used for the channel layer 11.

First, a case where a thin film material for the channel layer 11 is the group II oxide such as ZnO or the like will be described. For example, in the case of ZnO,

one can be selected from substrate materials described below.

First, for the substrate 16, for example, a material containing $LnABO_4$ for a basic structure (crystal group having a composition of $LnABO_4$, and a structure of $YbFe_2O_4$) like that described below can be used. That is, $LnABO_4$

Here, Ln: rare earth element of Sc, In, Lu, Yb, Tm, Ho, Er, Y or the like

A: Fe, Ga or Al

B: Mn, Co, Fe, Zn, Cu, Mg or Cd

The lattice constant of such a substrate material is set in the range of about 3.2 to 3.5Å. A material for such a basic structure is, e.g., $ScAlMgO_4$ or the like.

Fig. 3 shows a relation between a lattice constant and an ionic radius regarding $LnABO_4$. An abscissa indicates an ionic radius of an Ln oxide having a coordination number of 6, while an ordinate indicates a lattice constant. As shown, by analyzing the lattice constant, it can be understood that as an ionic radius (atom size) of an Ln element is larger, a lattice constant of $LnABO_4$ is increased. In addition, the lattice constants of ZnO, GaN and AlN are indicated by a horizontal line (broken line), and an oxide containing $LnABO_4$ near such a lattice constant for a basic structure is shown.

Fig. 4 shows an example of a substrate material containing $LnABO_4$ for a basic structure, and the lattice constant thereof. As exemplary materials having relatively small lattice constants, $ScAlMgO_4$, $ScAlZnO_4$, $ScAlCoO_4$, $ScAlMnO_4$, $ScGaZnO_4$, and $ScGaMgO_4$ are shown. Since the lattice constant of ZnO is 3.249Å as

shown in Fig. 2, if any one of the substrate materials shown in Fig. 6 is used, compatibility of the lattice constants can be improved. As substrate materials having high compatibility, $ScAlCuO_4$, $InAlMgO_4$, and so on, shown in Fig. 3 are available, and there should be no limitation in this regard.

Further, for the substrate 16, in order to realize matching with ZnO, a ZnO added oxide material like that described below can also be used. To use a general formula, a material (crystal group having a composition of $LnAO_3(BO)_n$, and a structure of $Yb_2Fe_3O_7$) containing $LnAO_3(BO)_n$ described below for a basic structure can be used as occasion demands. That is,

$LnAO_3(BO)_n$

Here, Ln: rare earth element selected from Sc, In, Lu, Yb, Tm, Ho, Er, Y, and so on

A: Fe, Ga or Al

B: Mn, Co, Fe, Zn, Cu, Mg or Cd

Thus, if ZnO is mixed in the $LnABO_4$ structure, the ZnO enters a lattice space, thus making it possible to synthesize a material approximated to the lattice constant of ZnO. If n is infinitely increased, the lattice constant endlessly approaches 3.249 (lattice constant of ZnO).

Fig. 5 shows a relation between a lattice constant and an ionic radius regarding $LnAO_3(BO)_n$. An abscissa indicates an ionic radius of an Ln oxide having a coordination number of 6, while an ordinate indicates a lattice constant. As in the case shown in Fig. 3, the analysis of the lattice constant shows that as an ionic radius (atom size) of an Ln element is larger, a lattice constant of $LnAO_3(BO)_n$ is increased. The lattice

constants of ZnO, GaN and AlN are indicated by a horizontal line (broken line), and an oxide containing $LnAO_3(BO)_n$ near such a lattice constant for a basic structure is shown.

As shown, specifically, lattice compatibility is improved by using, e.g., one of the followings:

$ScAlO_3(ZnO)_n$

$ScFeO_3(ZnO)_n$

$ScGaO_3(ZnO)_n$

$InFeO_3(ZnO)_n$

$InGaO_3(ZnO)_n$

$InAlO_3(ZnO)_n$

$YbAlO_3(ZnO)_n$

$LuAlO_3(ZnO)_n$

Further, among the above, a material can be selected from, e.g., the group consisting of $ScAlZn_3O_6$, $ScAlZn_4O_7$ and $ScAlZn_7O_{10}$, the group consisting of $ScGaZn_3O_6$, $ScGaZn_5O_8$ and $ScGaZn_7O_{10}$, the group consisting of $ScFeZn_2O_5$, $ScFeZn_3O_6$ and $ScFeZn_6O_9$, or the like.

Secondly, a case where a thin film material for the channel layer 11 is the group III nitride such as GaN, AlN or the like will be described. For example, as shown in Fig. 2, the lattice constants of GaN and AlN are respectively 3.112 Å and 3.189 Å. An oxide crystal taking the $LnABO_4$ structure shown in Figs. 3 and 4 has a lattice constant of about 3.2Å at a minimum. Thus, a crystal which can match the lattice constants of GaN and AlN may be selected from, among others, e.g., $ScAlMgO_4$, $ScAlZnO_4$, and so on, having smallest lattice constants.

Other than the materials shown in Figs. 3 to 5, the followings can be cited as materials having relatively

small lattice constants and high compatibility with GaN, AlN or the like:

$ScAlBeO_4$

$ScBMgO_4$

$ScBBeO_4$

In the above general formula $LnAO_3(BO)_n$, a material selecting Mg as B has high compatibility. In other words, this substrate is one obtained by adding MgO to one of the foregoing oxide substrate materials.

A proper insulating material is used for the gate insulating layer 15. For the gate insulating layer 15, a highly insulating material having high lattice compatibility with the material of the channel layer 11. As described above, similar to the case where the material having high lattice constant compatibility was used for the substrate 16 according to the thin film material of the channel layer 11, a proper insulting layer 15 having high lattice compatibility can be selected. For example, if ZnO is used for the channel layer 11, then, e.g., $ScAlMgO_4$ or the like can be used for the gate insulating layer 15. In addition, for the gate insulating layer 15, a transparent insulating material such as insulating ZnO doped with, e.g., an element capable of taking valence of 1 value or a group V element can also be used. As the element taking valence of 1 value, e.g., group I elements (Li, Na, K, Rb and Cs), Cu, Ag, Au, and so on, are available. As the group V element, N, P, As, Sb, Bi, and so on, are available. For both layers, lattice constants within all the surfaces coincide with one another at 1% or lower. Accordingly, mutual epitaxial growth is possible, thereby realizing a semiconductor device having superior lattice compatibility.

In addition, by using a ferroelectric material for the gate insulating layer 15, the transistor itself can be provided with a memory function. As ferroelectric materials, e.g., $Zn_{1-x}Li_xO$, $Zn_{1-x}(Li_yMg_{x-y})O$, and so on, are available. For the gate insulating layer 15, e.g., an insulator such as glass, vinyl, plastic or the like may be used. Other than these, for the gate insulating layer 15, an insulating oxide such as Al_2O_3, MgO, CeO_2, SiO_2 or the like can be used.

The gate insulating layer 15 has been described. For forming other proper insulating layers, the same materials can be used. Thus, it is possible to manufacture a semiconductor device having high lattice compatibility.

For the source 12, the drain 13 or the gate 14, a proper electrode material can be used. As such an electrode material, a conductive material doped/undoped with impurities as occasion demands, using the same material as that for the channel layer 11 as a base, can be used. As an electrode containing ZnO or the like as a base, conductive ZnO or the like is used, which is doped with, e.g., one selected from group III elements (B, Al, Ga, In, and Tl), group VII elements (F, Cl, Br, and I), group I elements (Li, Na, K, Rb and Cs) and group V elements (N, P, As, Sb and Bi), or undoped with any of such various elements. Here, in the case of doping such an element, the amount of doping can be set as occasion demands (e.g., n^{++}-ZnO or the like doped with high concentration n type can be used, but there should be no limitation in this regard). By using as a base such a material having the same structure/composition as that for the channel layer 11 or the like, it is possible to

manufacture a semiconductor device having high lattice constant compatibility and high quality. Moreover, other than the above materials, metal such as Al, Cu or the like, or highly doped semiconductor polysilicon or the like can be used. Other materials can also be used for the source 12, the drain 13 or the gate 14, e.g., In_2O_3, SnO_2, $(In\text{-}Sn)O_x$, and so on.

(2) FET equipped with substrate having buffer layer

Figs. 6A and 6B are sectional views, each of which shows a semiconductor device according to the second embodiment of the invention. As shown in Fig. 6A, the semiconductor device of the second embodiment is for an FET, and comprises: a source 12; a drain 13; a gate 14; a gate insulating layer 15; a channel layer 17; a buffer layer 18; and a substrate 16.

If the channel layer 11 is in an undoped pure state, or slightly doped with impurities, a constitution like that shown in Fig. 1A is employed to realizing good compatibility between the lattice constants of the substrate 16 and the channel layer 11. On the other hand, according to the second embodiment, with regard to a case where a material doped with a considerable amount of impurities (e.g., about 10 to 20%) is used for the channel layer 17, or the like, the compatibility between the lattice constants can be further improved. Here, for such a purpose, the buffer layer 18 is provided between the substrate 16 and the channel layer 17.

For the channel layer 17, a material having a composition similar to that of the first embodiment. However, in the second embodiment, one doped with a relatively large amount of impurities can be used. For

the substrate 16, similarly to the case of the first embodiment, a material having high compatibility is used properly according to the channel layer 17. For the buffer layer 17, if group II oxide or group III nitride is used for the channel layer 17, then a slightly doped or undoped insulating material having the same composition as that of the channel layer 17 can be used. For example, if e.g., ZnO is used for the channel layer 17, for the buffer layer 17, an insulating material such as insulating ZnO or the like slightly doped with an element capable of taking valence of 1 value or a group V element, or an insulating semiconductor such as undoped pure insulating ZnO or the like, can be used. As the element taking valence of 1 value, e.g., group I elements (Li, Na, K, Rb, and Cs), Cu, Ag, Au, and so on, are available. As the group V element, N, P, As, Sb, Bi, and so on, are available. In the second embodiment, as in the case described above with reference to the first embodiment, the combination of each materials for the channel layer 17, for the buffer layer 18 with the same materials in composition as the thin film material of the channel layer 17, and for the substrate 16 can be properly selected by considering the compatibility of the lattice constants.

(3) Characteristic of semiconductor device

Next, description will be made of a suitable example of the invention, by making comparison in characteristics between the ZnO thin film formed on the $ScAlMgO_4$ substrate of the first embodiment and the ZnO thin film formed on the conventional sapphire substrate. In this example, the ZnO film was formed by using laser

molecular beam epitaxy or pulse laser deposition at a substrate temperature of 300 to 1000℃.

Fig. 7 illustrates in comparison electric characteristics of a zinc oxide thin film and a zinc oxide bulk single crystal. Fig. 7 specifically shows the comparison of electric characteristics between a case where zinc oxide thin films are respectively formed on the $ScAlMgO_4$ substrate and the sapphire substrate (α-Al_2O_3 substrate) and a case where a zinc oxide bulk single crystal is prepared by hydrothermal synthesis. As an electric characteristic, a relation between mobility μ and donor concentration N_D indicating electron or carrier concentration at a room temperature is shown.

A relation between resistivity ρ and mobility μ/donor concentration N_D is as follows:

$\rho=1/(e\mu N_D)$

Here, e represents an elementary charge quantity.

The characteristic of a bulk single crystal is shown to indicate the original physical property of ZnO. The bulk ZnO single crystal has high mobility, low donor concentration and a good characteristic. One of the objects of invention is to obtain a characteristic as close as possible to such a bulk single crystal characteristic. On the other hand, if the ZnO film is formed on the conventional sapphire substrate, mobility is low, and donor concentration is high. In the case of the ZnO film formed on the $ScAlMgO_4$ substrate of the invention, however, compared with the conventional case, mobility is high, and donor concentration is low, thus making it possible to obtain a good characteristic approximated to that of the ZnO bulk single crystal. Further, as shown, the concentration of donor to be mixed in is low from the

beginning according to the invention. Thus, by adjusting the amount of donor or acceptor to be added, a control range/setting range can be set large for donor concentration or acceptor concentration. According to the invention, it is possible to form a thin film having carrier concentration of about $10^{15}cm^{-3}$ and electron mobility of about 60 to $70cm^2/Vs$ with good reproducibility. Such a difference in characteristic may be attributed to defects, impurities, grain boundaries or the like.

As apparent from Fig. 7, a high switching speed can be achieved by applying the invention to a transistor or the like. Moreover, since the application of the invention to the FET or the like results in a wider depletion layer when an electric field is applied, a gate voltage for switching can be low. By applying the invention to the light emission device, it is possible to increase light emission efficiency.

Fig. 8 illustrates in comparison X-ray reciprocal lattice mapping between the zinc oxide thin film and the zinc oxide bulk single crystal. Fig. 8 specifically shows the comparison of X-ray reciprocal lattice mapping between a case where ZnO thin films are formed respectively on the $ScAlMgO_4$ substrate and the sapphire substrate, and a case where a ZnO thin film having a zinc oxide bulk single crystal formed by hydrothermal synthesis is formed. In the drawing, a reciprocal lattice space between the reciprocal number Qz (ordinate) of the lattice constant of a z direction and a reciprocal number Qx (abscissa) of the lattice constant of an x direction is also shown. In shown arrow directions, (a) a reciprocal number of grain size, (b) fluctuation of lattice plane

spacing, and (c) fluctuation of lattice plane direction (mosaicness) are respectively shown. Here, the characteristic of ZnO (114) is shown as an example of asymmetrical diffraction surfaces. Similar results can be obtained for each diffraction surfaces (115), (104) and (105).

As shown, according to the invention, compared with the conventional case, the followings are apparent, i.e., (a) a grain size is larger, (b) fluctuation of lattice plane space is smaller, and (c) fluctuation of a lattice plane direction is smaller (mosaicness). In addition, according to the invention, compared with the conventional case, crystallinity can be improved drastically, and a single crystal ZnO thin film similar in mosaicness, a grain size, and so on, to the bulk single crystal, can be obtained. Apparently from the drawing, according to the invention, the lattice constant has been approximated to that of a bulk crystal, and diffraction peak has become sharp.

Fig. 9 is a comparative view illustrating the dependence of the half value width of an X-ray rocking curve on a substrate temperature. In the drawing, a relation between a half value width and a deposition temperature regarding the ZnO films on the $ScAlMgO_4$ substrate and the sapphire substrate.

Generally, the half value width of an X-ray rocking curve indicates the fluctuation of a lattice plane direction (mosaicness) and a gain size. Specifically, according to the invention, since the half value width of the X-ray rocking curve is smaller compared with that of the conventional case, the ZnO films have superior characteristics. For example, if the $ScAlMgO_4$ substrate

is used as in the case of the invention, even for a ZnO thin film formed at a low deposition temperature of about 300°C, mosaicness and a grain size similar to those of the thin film deposited on the conventional sapphire substrate at 1000°C are obtained, thus making it possible to obtain a thin film having very high crystallinity. Generally, interlayer diffusion may occur if a thin film is formed at a high temperature. According to the invention, however, such interlayer diffusion can be reduced or even prevented.

Fig. 10 is a comparative view illustrating the flatness of a thin film surface. As apparent from the drawing, the ZnO thin film surface on the $ScAlMgO_4$ of the invention has concave and convex portions greatly reduced (e.g., about 1/100 by precise measurement) compared with those on the ZnO thin film surface on the conventional sapphire substrate. According to the invention, the ZnO thin film surface can be formed flat atomically by the step of 0.26nm (1/2 of c axis length) or 0.52nm (c axis length).

Fig. 11 is a comparative view illustrating the dependence of nitrogen concentration on a substrate temperature. Fig. 11 specifically shows a relation between nitrogen concentration and a deposition temperature regarding a case where ZnO thin films doped with nitrogen are formed on the $ScAlMgO_4$ substrate of the invention and the conventional sapphire substrate. According to the invention, compared with the conventional case, the amount of nitrogen doping can be almost doubled (in other words, nitrogen doping is easier). This means that to obtain the amount of doping similar to that of the conventional case, a ZnO thin film

can be formed at a low deposition temperature of about 50°C, in other words, a doping characteristic can be improved. The nitrogen doping characteristic is equivalent to the acceptor characteristic of the device.

(3') Other FET

Figs. 12A and 12B are sectional views, each of which shows a semiconductor device according to the third embodiment of the invention. The semiconductor device of the third embodiment shown in Fig. 12A is for an FET, and comprises: a channel layer 21; a source 22; a drain 23; a gate 24; a gate insulating layer 25; and a substrate 26. The source 22 and the drain 23 are formed on the substrate 26. The channel layer 21 is formed to cover these components. Further, the gate insulating layer 25 is formed on the channel layer 21. The gate 24 is formed on the gate insulating layer 25. The gate 24, the gate insulating layer 25 and the channel layer 21 make MIS structure.

Fig. 12B shows a modified example of the third embodiment. Different from the one shown in Fig. 12A, the gate insulating layer 25 is not formed, and the gate 24 and the channel layer 21 are coupled by Schottky junction. If the gate insulating layer 25 is formed as in the case shown in Fig. 12A, there is little limitation placed on a voltage applied to the gate. On the other hand, if the gate insulating layer 25 is not formed as in the case shown in Fig. 12B, a withstand voltage is lowered between the gate and the source, and between the gate and the drain. In this case, a manufacturing process is simple.

With such constitutions, as described above with

reference to the first and second embodiments, the thin film material of the channel layer 21, the source 22 or the drain 23, and the material of the substrate 26 or the gate insulating layer 25 can be properly combined to be used so that the lattice constants of both can be matched with each other.

Fig. 13 is a sectional view showing a semiconductor device according to the fourth embodiment of the invention. The semiconductor device of the fourth embodiment is for an FET, and comprises: a channel layer 31; a source 32; a drain 33; a gate 34; a gate insulating layer 35; and a substrate 36. The channel layer 31 is formed on the substrate 36. The gate insulating layer 35 is formed on the channel layer 31, and the gate 34 is formed on the gate insulating layer 35. The source 32 and the drain 33 can be formed by, for example, diffusion, ion implantation or the like, using the gate insulating layer 35 as a mask. In addition, by properly setting the size of the gate 34 as a modified example of the described embodiment, the gate insulating layer 35 can be omitted.

Also, with such constitutions, as described above with reference to the first and second embodiments, the thin film material of the channel layer 21 and the material of the substrate 26 or the gate insulating layer 35 can be properly combined to be used so that the lattice constants can be matched with each other. Further, as described above with reference to the second embodiment, a buffer layer can be added between the channel layer 31 and the substrate 36 according to the thin film material of the channel layer 31 and the doping amount of impurities.

In the foregoing third and fourth embodiments, if

not specified otherwise, materials similar to those of the first and second embodiments can be used for the respective components.

(4) Light emission device

Fig. 14 is a sectional view showing a semiconductor device according to the fifth embodiment of the invention. The semiconductor device of the fifth embodiment is for a light emission device such as a laser diode or the like, and comprises: a light emission layer 41; a p type semiconductor layer 42; an n type semiconductor layer 43; first and second electrodes 45 and 46; and a substrate 47.

The light emission layer 41 is held between the p type semiconductor layer 42 and the n type semiconductor layer 43. This light emission layer 41 can be formed by using, e.g., undoped ZnO, or of a very thin multilayer film containing (Mg, Zn)O and ZnO. In this case, the ZnO layer is called a well layer, and the (Mg, Zn)O layer is called a barrier layer. In addition, one having a bandgap of the barrier layer set larger than that of the well layer is used. As other materials for the light emission layer 41, the multilayer structure of (Zn, Cd)O and ZnO, the multilayer structure of (Mg, Zn)O and (Zn, Cd)O, and so on, are available. Further, for the light emission layer 41, a multilayer reflecting film, a double heterostructure, a surface emitting laser structure, and so on, can be properly employed, and combined to be used.

As base materials for the p type and n type semiconductor layers 42 and 43, materials similar to those of the first embodiment can be properly used. For

the p type semiconductor layer 42, for example, one may be selected from group II oxides such as a p type ZnO or the like, and group III nitrides such as p type GaN, AlN, InGaN, AlInN or the like. In the case of the p type ZnO, for example, ZnO is one doped with a group I element (Li, Na, K, Rb or Sc), or a group V element (N, P, As, Sb or Bi). For the n type semiconductor layer 43, for example, one may be selected from the group II oxides such as n type ZnO or the like, and the group III nitrides such as n type GaN, AlN or the like. In the case of the n type ZnO, for example, ZnO is one doped with a group III element (B, Al, Ga, In or Tl), or a group VII element (F, Cl, Br or I). The doping amount of each of such elements can be set properly according to a device dimension, a thickness, integration degree, performance or the like. As a material for the second electrode (n type electrode) 46, for example, one similar to that for the source 12, the drain 13 or the gate 14 of the foregoing first embodiment can be used. For the first electrode (p type electrode) 45, for example, an ohmic electrode containing Au, Pt, and Ni/Ti (multilayer structure) or the like can be used.

With such constitutions, as described above with reference to the first embodiment, the thin film material of the n type semiconductor layer 43 (p type semiconductor layer if the semiconductor layer joined to the substrate 47 is a p type) and the material of the substrate 47 can be properly combined to be used such that the lattice constants of both can be matched with each other. Further, as described above with reference to the second embodiment, a buffer layer can be added between the n type semiconductor layer 43 and the substrate 47 according to the thin film material of the n

type semiconductor layer 43 and the doping amount of impurities. By using a combination of materials having high lattice compatibility for all or part of the p type semiconductor layer 42, the n type semiconductor layer 43, the light emission layer 41 and the substrate 47, it is possible to manufacture a high quality semiconductor device.

In the foregoing fifth embodiment, if not specified otherwise, materials similar to those of the first and second embodiments can be used for the respective components. In addition, by using a transparent semiconductor, a light can be emitted from the light emission layer toward the upper or lower surface of the drawing. Apparently, the invention can be applied to various light emission devices including a surface emitting laser, an electroluminescence device, and so on.

(5) Surface Acoustic Wave (SAW) device

Figs. 15A and 15B are constitutional views, each of which shows a semiconductor device according to the sixth embodiment of the invention. Specifically, Fig. 15A is a perspective view of a SAW device; Fig. 15B is a sectional view taken on line B-B' of Fig. 15A.

The SAW device comprises: a substrate 111; a semiconductor layer 112; and input and output electrodes 113 and 114. The SAW device is a semiconductor device designed to output a proper signal from the output electrode 114 based on the filter characteristic thereof when a high frequency signal is entered from the input electrode 113.

The semiconductor layer 112 is an insulating semiconductor, and a material similar to that of the first

embodiment can be properly used as a base. For the semiconductor layer 112, for example, insulating ZnO undoped/doped with a group I or III element can be used. To suppress grain boundaries, for example, IIId transition metal (Co, Ni or the like) may be slightly added as impurities.

With such a constitution, as described above with reference to the first and second embodiments, the thin film material of the semiconductor layer 112 and the material of the substrate 111, the input electrode 113 and the output electrode 114 can be properly combined to be used so that the lattice constants of both can be matched with each other.

(6) Other applications

The present invention is very advantageous when applied to a laminated semiconductor device, since the surface of each layer can be formed to be very flat. In this case, the foregoing materials can be properly selected for lamination by considering compatibility between the lattice constants of each layer and a layer to be joined thereto. In addition, a plurality of transistors may be selected, and mixed for lamination.

In addition to the SAW device, the invention can be applied to an optical waveguide, an optical integrated circuit such as a diffraction grating or the like, and an optical device. The invention can also be applied to various sensors including a varistor, a humidity sensor, a temperature sensor, a gas sensor, and so on. The invention can even be applied to a memory. If the invention is applied to the memory, a memory device can be realized by arraying transistors and capacitors in a

matrix form, and using each transistor to drive each capacitor. In addition, according to the invention, the proper devices including the transistor, the light emission device, the capacitor, and so on, can be formed on the same substrate. Moreover, by forming a high quality crystal, the invention can be widely applied to the semiconductor devices in many fields.

The size, thickness, dimension, or the like of the semiconductor device and the respective layers can be properly designed according to use, a process or the like. The amount of doping can be set properly according to a need, e.g., a manufacturing process, device performance or the like.

As the n and p type semiconductors and the conductive and insulating materials, the example of the semiconductor containing ZnO as a base and doped with each element was described. However, the invention is not limited to this example. In the first and second embodiments, the channel layers were formed on the substrates. However, as apparent from the other embodiments, other than the channel layer, an insulating or conductive semiconductor layer, a doped or undoped semiconductor layer, or an n or p type semiconductor layer can be formed on the substrate as occasion demands.

INDUSTRIAL APPLICABILITY

According to the present invention, since the thin film material such as group II oxide, e.g., ZnO, group III nitride, e.g., GaN, or the like, and the oxide crystal having very high lattice compatibility are used for the substrate, the quality of the thin film material can be

greatly improved. Thus, it is possible to form a thin film having high quality comparable to a bulk single crystal, and to manufacture a semiconductor device having superior characteristics. Moreover, according to the invention, it is possible to form a semiconductor thin film of ZnO, GaN or the like, having almost no grain boundaries, a large grain size, small fluctuation of lattice plane spacing, very small mosaicness, and high quality substantially comparable to a single crystal.

According to the invention, since the lattice mismatching of, e.g., $ScAlMgO_4$(SCAM) crystal or the like with respect to ZnO is small (about 0.13%), a ZnO thin film of substantially a single crystal can be formed on the substrate. Moreover, according to the invention, compared with the conventional case of using the sapphire substrate or the like, ZnO on the SCAM substrate has high electron mobility, and can be approximated to a ZnO single crystal.

According to the invention, by combining ZnO as a transparent semiconductor material with the transparent highly insulating SCAM substrate, it is possible to manufacture a transparent semiconductor device, and to greatly improve the performance of the heterostructured device. Moreover, transparent materials may be properly used for part or all of various electrode materials, the insulating layers, and so on, in the FET or the like.

By applying the invention to the transistor or the like, it is possible to achieve a high switching speed. By applying the invention to the field effect transistor or the like, a depletion layer is enlarged when an electric field is applied. Thus, a gate voltage for switching can

be reduced. In addition, by applying the invention to the light emission device, light emission efficiency can be increased.

Furthermore, the invention can be applied to the field effect transistor or the bipolar transistor, the GaN based light emission device (LED, laser) containing a nitride blue laser, the Surface Acoustic Wave (SAW) device, and various electronic devices including a sensor, and so on, and it is possible to improve the performance thereof.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate using a material containing one selected from $LnABO_4$ and $LnAO_3(BO)_n$ for a basic structure (where Ln: rare earth element selected from Sc, In, Lu, Yb, Tm, Ho, Er, Y or the like, A: selected from Fe, Ga and Al, and B: selected from Mn, Co, Fe, Zn, Cu, Mg and Cd); and

a semiconductor layer formed on said substrate by using a material selected from group II oxides such as zinc oxide ZnO, zinc magnesium oxide $Mg_xZn_{1-x}O$, zinc cadmium oxide $Cd_xZn_{1-x}O$, cadmium oxide CdO or the like.

2. The semiconductor device according to claim 1, wherein as a material for said substrate, one selected from groups consisting of $ScAlMgO_4$, $ScAlZnO_4$, $ScAlCoO_4$, $ScAlMnO_4$, $ScGaZnO_4$ and $ScGaMgO_4$, $ScAlZn_3O_6$, $ScAlZn_4O_7$ and $ScAlZn_7O_{10}$, $ScGaZn_3O_6$, $ScGaZn_5O_8$ and $ScGaZn_7O_{10}$, and $ScFeZn_2O_5$, $ScFeZn_3O_6$ and $ScFeZn_6O_9$ is used, and ZnO is used as a material for said semiconductor layer.

3. The semiconductor device according to claim 1, wherein as a material for said substrate, one selected from groups consisting of $ScAlO_3(ZnO)_n$, $ScFeO_3(ZnO)_n$, $ScGaO_3(ZnO)_n$, $InFeO_3(ZnO)_n$, $InGaO_3(ZnO)_n$, $InAlO_3(ZnO)_n$, $YbAlO_3(ZnO)_n$ and $LuAlO_3(ZnO)_n$ is used, and ZnO is used as a material for said semiconductor layer.

4. A semiconductor device comprising:

a substrate using a material containing one selected from $ScAlBeO_4$, $ScBMgO_4$, $ScBBeO_4$ and $lnAO_3(MgO)_n$ (here, A: selected from Fe, Ga and Al) for a basic structure; and

a semiconductor layer formed on said substrate by using a material selected from groups consisting of GaN, AlN, InGaN and AlInN.

5. The semiconductor device according to any one of claims 1 to 4, further comprising: a buffer layer, between said substrate and said semiconductor layer, using an insulating material by using a material having a composition or a structure identical to that of said semiconductor layer as a base and slightly doped or undoped with impurities.

6. The semiconductor device according to claim 5, wherein ZnO is used for said semiconductor layer and, for said buffer layer, one selected from an insulating material such as insulating ZnO or the like slightly doped with an element capable of taking valence of 1 value or a group V element, and an insulating semiconductor containing undoped and pure insulating ZnO, is used.

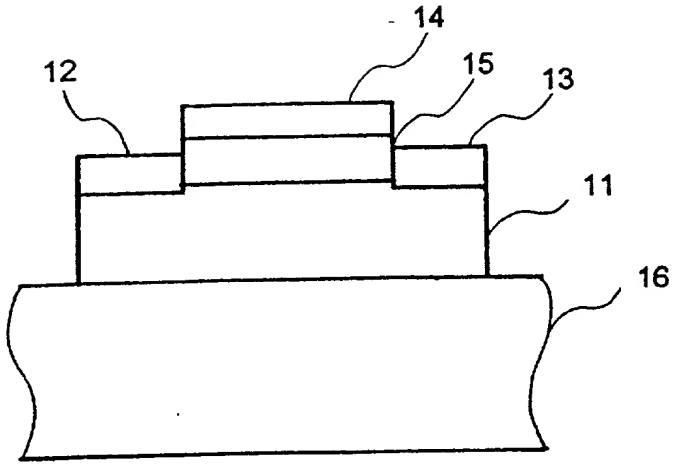
7. The semiconductor device according to any one of clams 1 to 6, further comprising an insulating layer formed by using a material identical to that for said substrate for a basic structure.

8. The semiconductor device according to any one of claims 1 to 7, further comprising: a light emission layer formed on said semiconductor layer by using a material having a composition or a structure identical to that of said semiconductor layer as a base; and a second semiconductor layer which is formed on said light

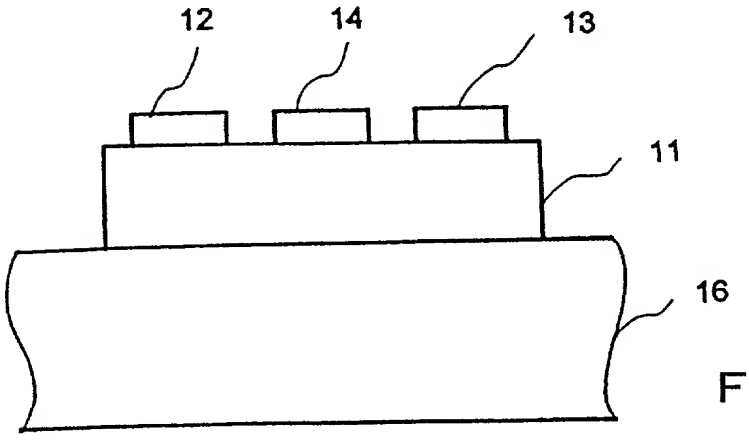
emission layer by using a material having a composition or a structure identical to that of said semiconductor layer as a base, and which has a different channel from that of said semiconductor layer.

9. The semiconductor device according to claim 8, wherein for said light emission layer, one selected from a multilayer structure of (Mg, Zn)O and ZnO, a multilayer structure of (Zn, Cd)O and ZnO, and a multilayer structure of (Mg, Zn)O and (Zn, Cd)O, is used.

10. The semiconductor device according to any one of claims 1 to 7, wherein said semiconductor layer is an insulating semiconductor, input and output electrodes are further formed on said semiconductor layer, and a filter characteristic is provided.



(A)



(B)

FIG. 1

THIN FILM MATERIAL	LATTICE CONSTANT (Å)
ZnO	3.249
AlN	3.112
GaN	3.189
InN	5.76

FIG. 2

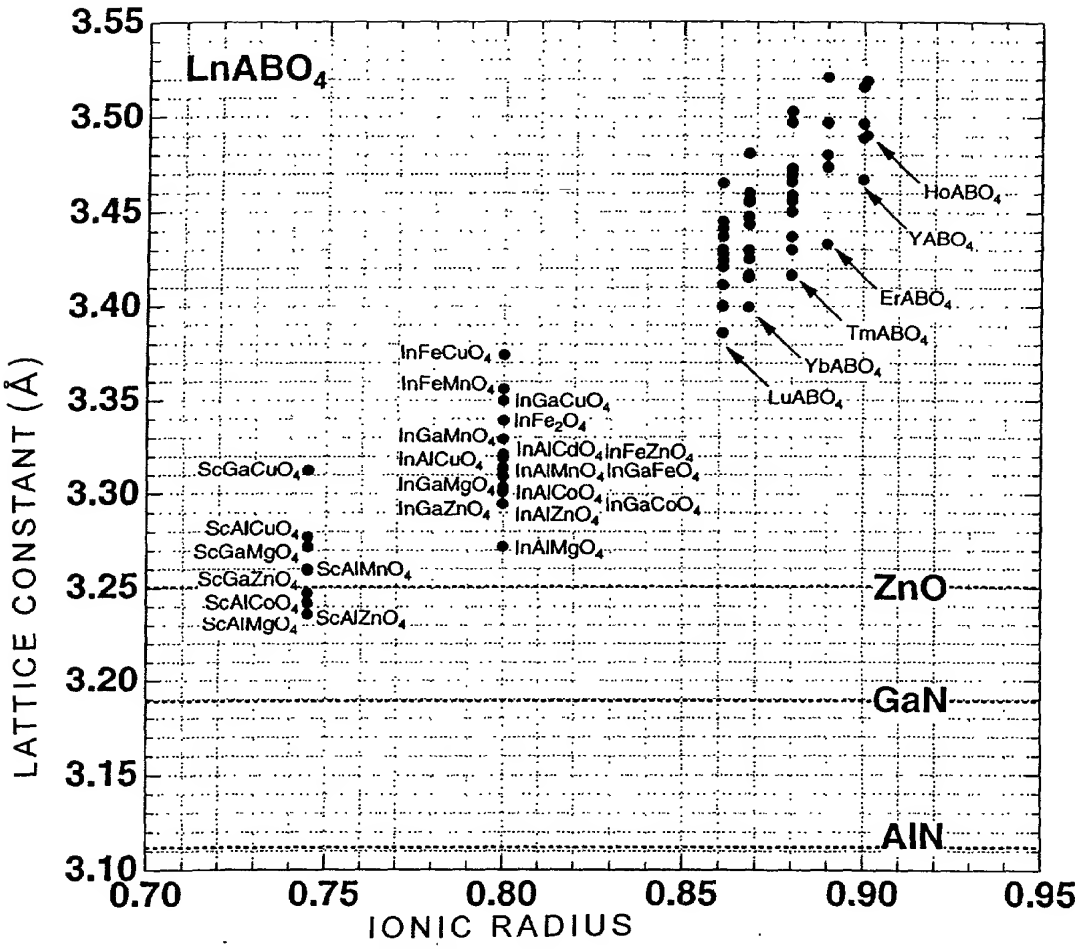
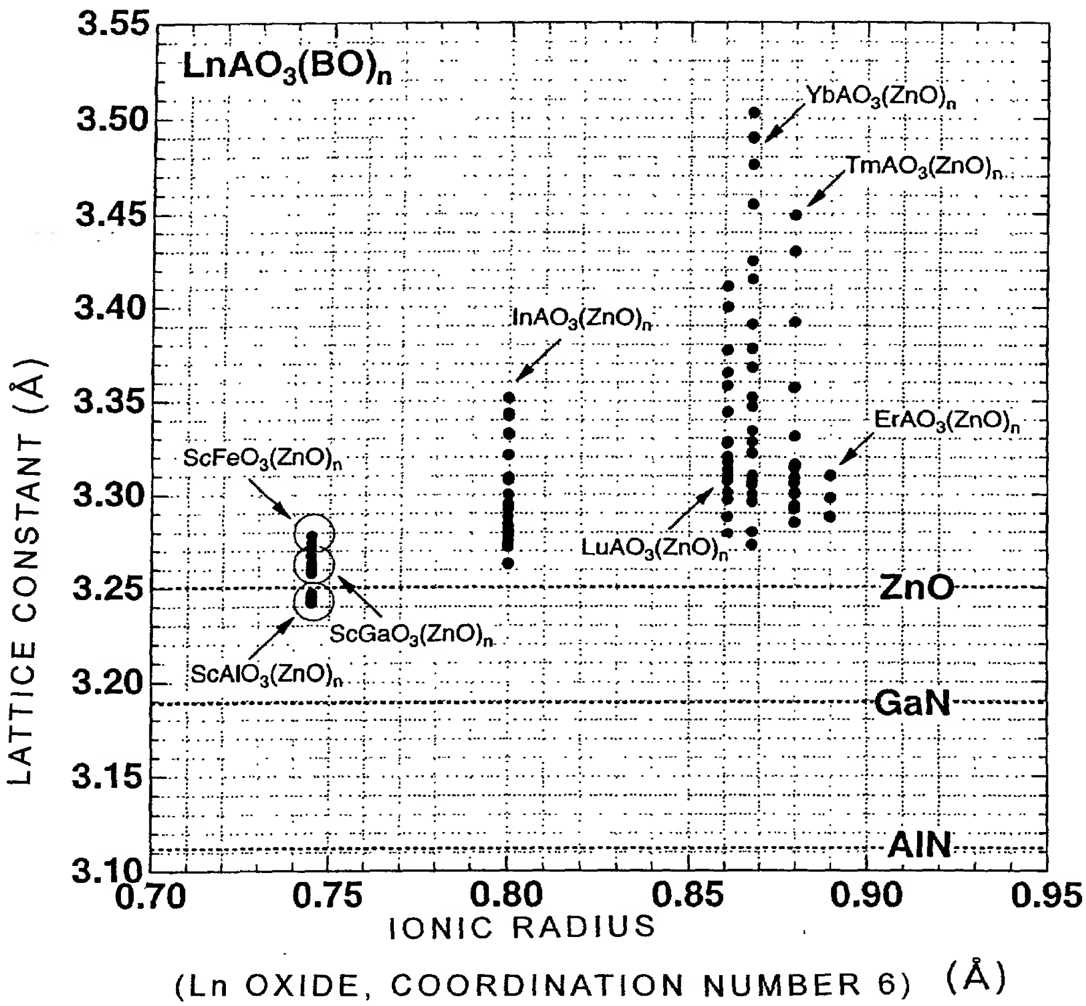

LnABO4
HoABO4
YABO4
ErABO4
TmABO4
YbABO4
LuABO4
InFeCuO4
InFeMnO4
InGaCuO4
InFe2O4
InGaMnO4
InAlCuO4
InAlCdO4
InFeZnO4
InAlMnO4
InGaFeO4
InGaMgO4
InAlCoO4
InGaCoO4
InGaZnO4
InAlZnO4
InAlMgO4
ScGaCuO4
ScAlCuO4
ScGaMgO4
ScAlMnO4
ScGaZnO4
ScAlCoO4
ScAlMgO4
ScAlZnO4
ZnO
GaN
AlN
LATTICE CONSTANT (Å)
3.55
3.50
3.45
3.40
3.35
3.30
3.25
3.20
3.15
3.10
0.70
0.75
0.80
0.85
0.90
0.95
IONIC RADIUS
(Ln OXIDE, COORDINATION NUMBER 6) (Å)

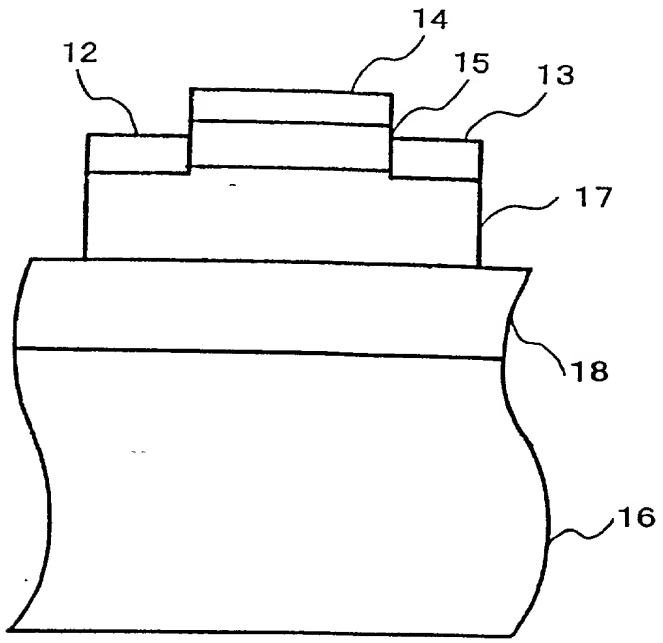
FIG. 3

SUBSTRATE MATERIAL	LATTICE CONSTANT(Å)
$ScAlMgO_4$	3.236
$ScAlZnO_4$	3.242
$ScAlCoO_4$	3.247
$ScAlMnO_4$	3.260
$ScGaZnO_4$	3.259
$ScGaMgO_4$	3.272

FIG. 4


LnAO3(BO)n
YbAO3(ZnO)n
TmAO3(ZnO)n
InAO3(ZnO)n
ErAO3(ZnO)n
ScFeO3(ZnO)n
LuAO3(ZnO)n
ZnO
ScGaO3(ZnO)n
ScAlO3(ZnO)n
GaN
AlN
3.55
3.50
3.45
3.40
3.35
3.30
3.25
3.20
3.15
3.10
0.70
0.75
0.80
0.85
0.90
0.95
LATTICE CONSTANT (Å)
IONIC RADIUS
(Ln OXIDE, COORDINATION NUMBER 6) (Å)

F I G. 5



(A)

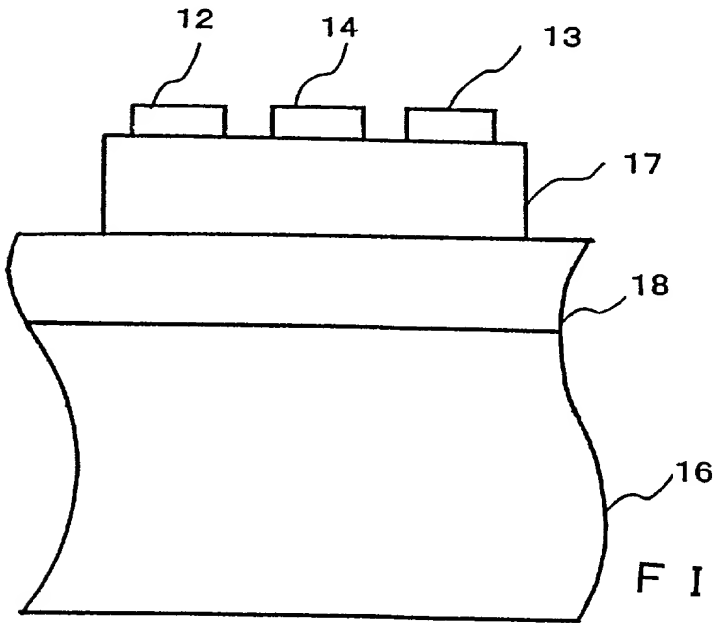


FIG. 6

(B)

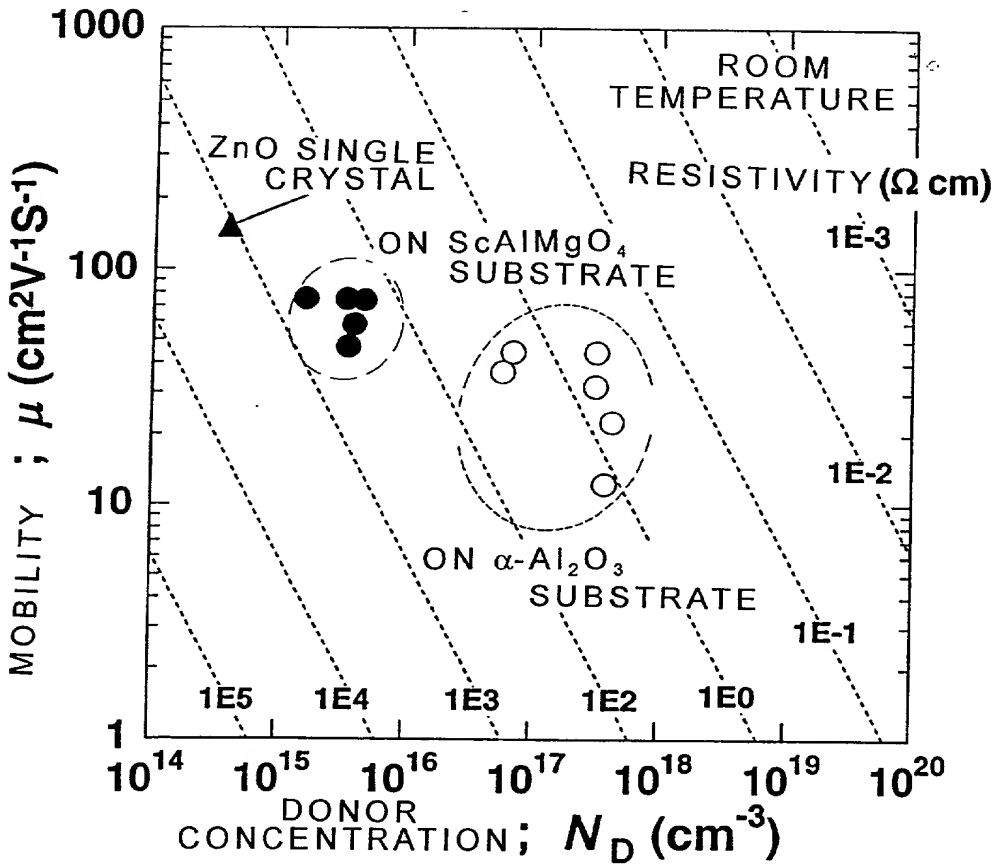

1000
100
10
1
MOBILITY ; μ (cm²V⁻¹S⁻¹)
ROOM
TEMPERATURE
ZnO SINGLE
CRYSTAL
RESISTIVITY (Ω cm)
ON ScAlMgO₄
SUBSTRATE
1E-3
1E-2
ON α-Al₂O₃
SUBSTRATE
1E-1
1E5
1E4
1E3
1E2
1E0
10¹⁴
10¹⁵
10¹⁶
10¹⁷
10¹⁸
10¹⁹
10²⁰
DONOR
CONCENTRATION; N_D (cm⁻³)

FIG. 7

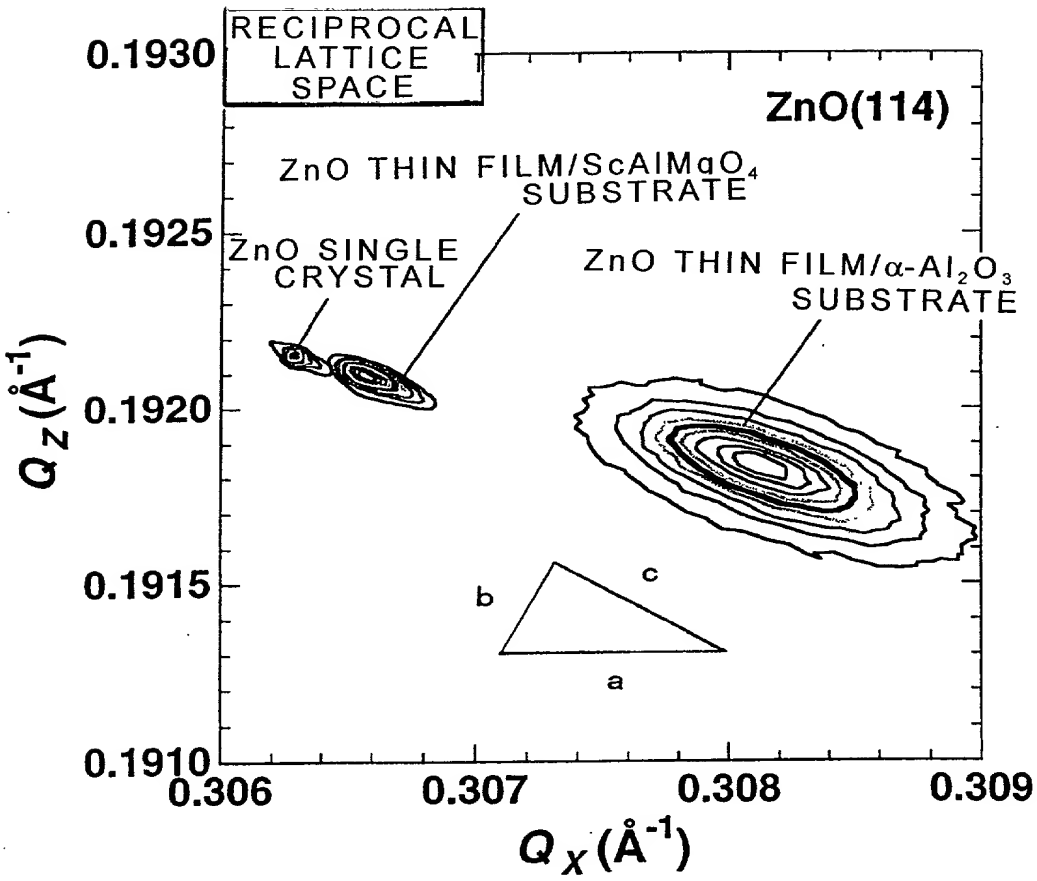


FIG. 8

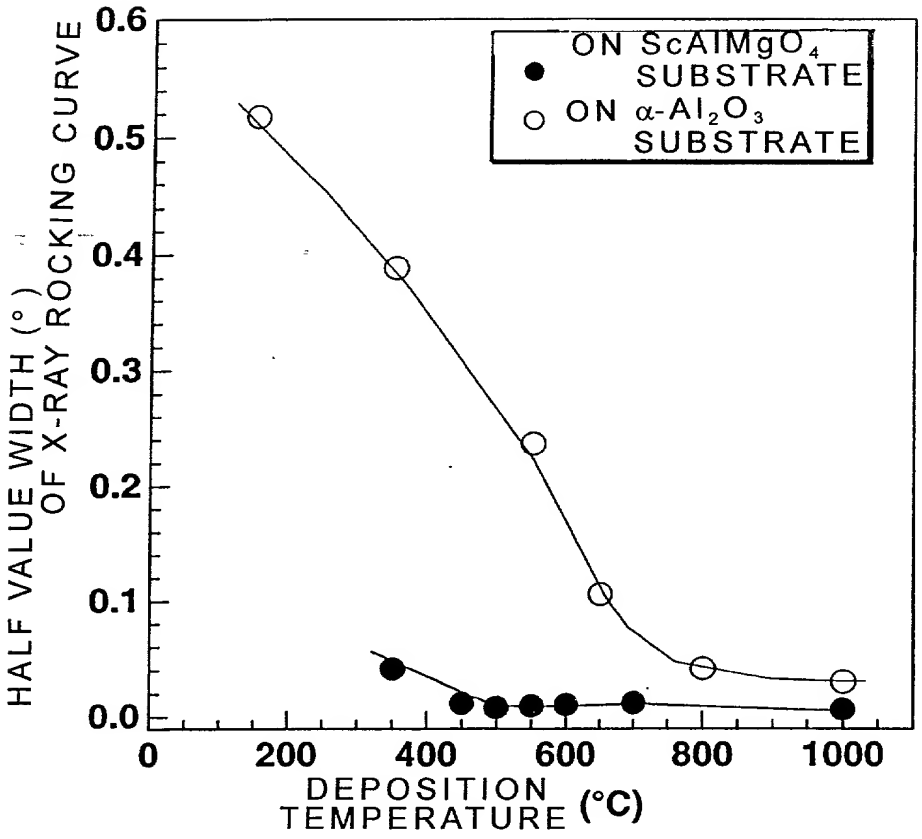

HALF VALUE WIDTH (°) OF X-RAY ROCKING CURVE
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
200
400
600
800
1000
DEPOSITION TEMPERATURE (°C)
ON ScAlMgO4 SUBSTRATE
ON α-Al2O3 SUBSTRATE

FIG. 9

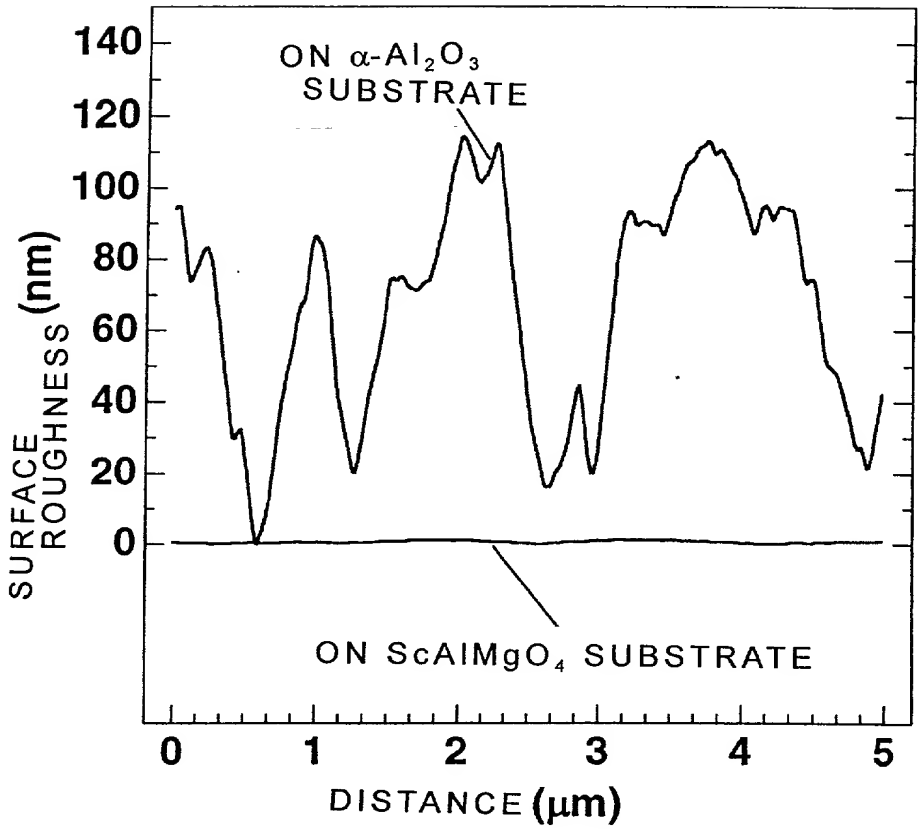

140
120
100
80
60
40
20
0
SURFACE ROUGHNESS (nm)
ON α-Al2O3 SUBSTRATE
ON ScAlMgO4 SUBSTRATE
0
1
2
3
4
5
DISTANCE (μm)

FIG. 10

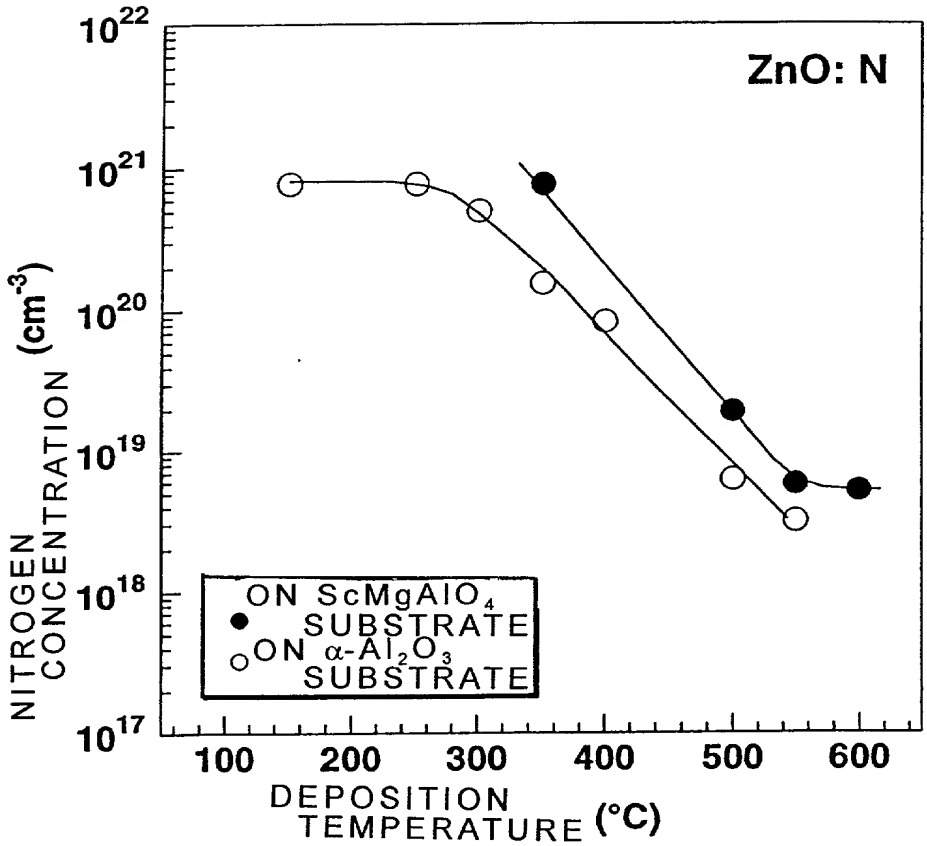
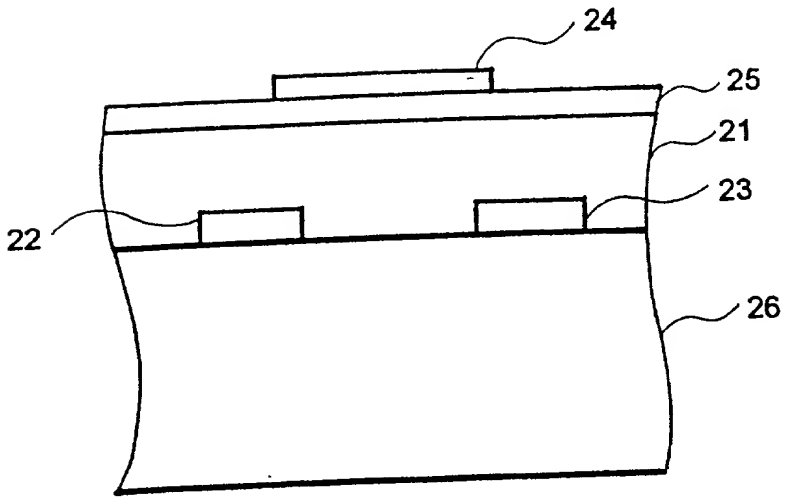
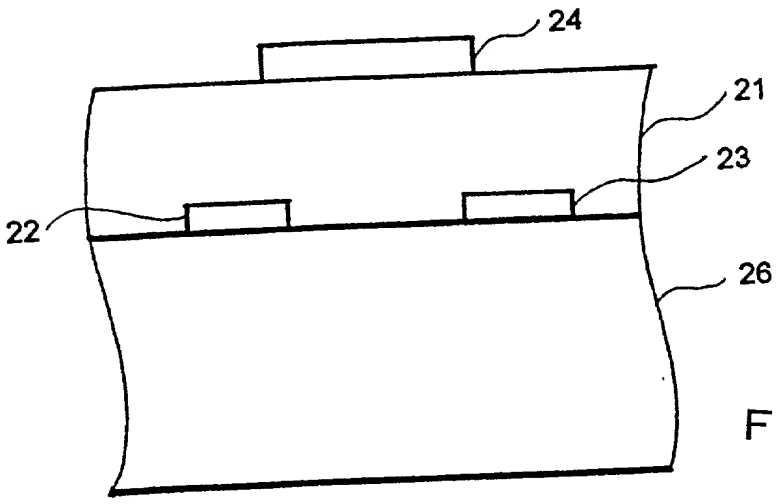

ZnO: N
NITROGEN CONCENTRATION (cm-3)
10^22
10^21
10^20
10^19
10^18
10^17
ON ScMgAlO4 SUBSTRATE
ON α-Al2O3 SUBSTRATE
100
200
300
400
500
600
DEPOSITION TEMPERATURE (°C)

FIG. 11



(A)



(B)

FIG. 12

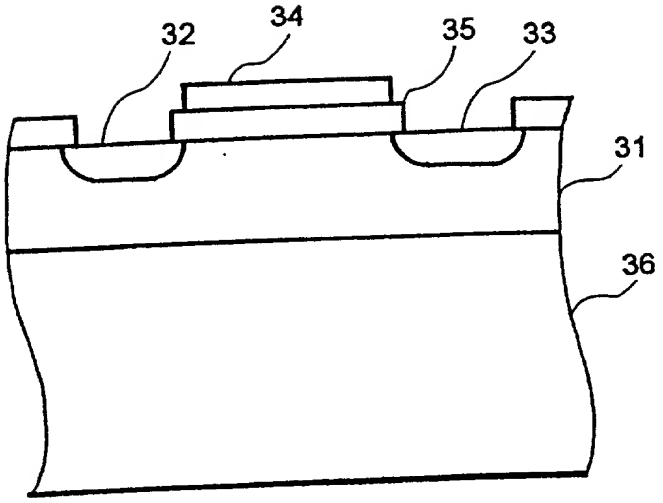


FIG. 13

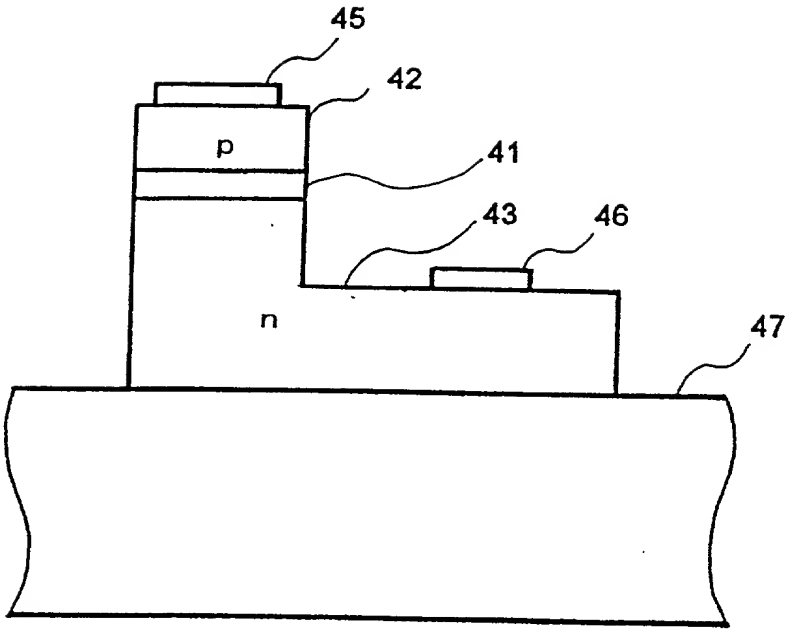
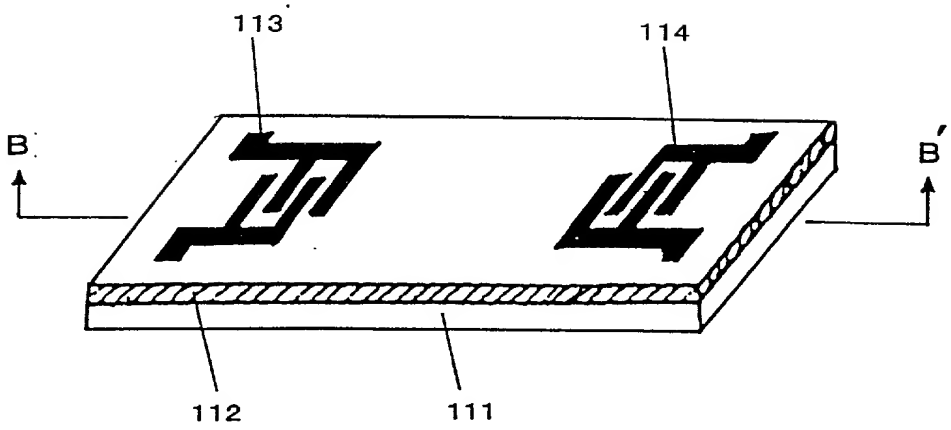
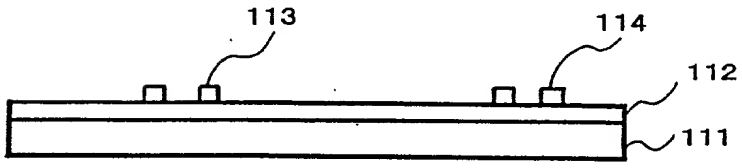


FIG. 14



(A)



(B)

FIG. 15

Declaration and Power of Attorney For Patent Application

#3

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

SEMICONDUCTOR DEVICE

上記発明の明細書は、

the specification of which

☐ 本書に添付されています。
☐ is attached hereto.

☒ ____月____日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

☒ was filed on 20 September 2001
as United States Application Number or
PCT International Application Number
09/926,186 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条（a）-（d）項又は365条（b）項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365（a）項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Claimed 優先権主張 Yes はい	No いいえ
11 82043	JAPAN	25 March 1999	☒	☐
			☐	☐

私は、第35編米国法典119条（e）項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条（c）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
PCT/JP00/01736	22 March 2000	

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
(弁護士、または代理人の指名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

022850

書類送付先

Send Correspondence to:

022850

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

(703) 413-3000

単独発明者または第一の共同発明者の氏名 1-CC	Full name of sole or first joint inventor Masashi KAWASAKI
発明者の署名 日付	Inventor's signature Date Oct 18, 2001
住所	Residence 4-2-5-116, Sagamiohno, Sagamihara-shi, Kanagawa 228-0803 JPX JAPAN
国籍	Citizenship JAPAN
郵便の宛先	Post Office Address same as above
第二の共同発明者の氏名 2-CC	Full name of second joint inventor, if any Hideo OHNO
第二の共同発明者の署名 日付	Second joint Inventor's signature Date Oct. 18, 2001
住所	Residence 3-33-10, Katsura, Izumi-ku, Sendai-shi, Miyagi 981-3134 JPX JAPAN
国籍	Citizenship JAPAN
郵便の宛先	Post Office Address same as above

(第三以降の共同発明者についても同様に記載し、署名すること)

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Declaration
(日本語宣言書)

第三の共同発明者の氏名 3-00	Full name of third joint inventor, if any Akira OHTOMO
第三の共同発明者の署名 日付	Third joint Inventor's signature Date Akira Ohtomo Oct 22 2009
住所	Residence 3-24-14-103, Chuorinkan, Yamato-shi, Kanagawa 242-0007 JPX JAPAN
国籍	Citizenship JAPAN
郵便の宛先	Post Office Address same as above

第四の共同発明者の氏名	Full name of fourth joint inventor, if any
第四の共同発明者の署名 日付	Fourth joint Inventor's signature Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

第五の共同発明者の氏名	Full name of fifth joint inventor, if any
第五の共同発明者の署名 日付	Fifth joint Inventor's signature Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

第六の共同発明者の氏名	Full name of sixth joint inventor, if any
第六の共同発明者の署名 日付	Sixth joint Inventor's signature Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

(第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。)

(Supply similar information and signature for third and subsequent joint inventors.)